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10/714,780	11/17/2003	Wanmo Wong	400.233US01	2431
27073 7590 02/08/2007 LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			EXAMINER FLOURNOY, HORACE L	
			ART UNIT 2189	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/714,780	Applicant(s) WONG ET AL.	
	Examiner Horace L. Flournoy	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 October 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,5-11,13-33,35-40 and 42-44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-11,13-33,35-40 and 42-44 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed October 13th 2006. Claims 1,2,5-11,13-33, 35-40 and 42-44 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,5-11,13-33, 35-40 and 42-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Sekine (U.S. Patent Number 5,896,398 hereafter referred to as Sekine) with Microsoft Computer Dictionary (MSCD), 5th edition offered as extrinsic evidence.

With respect to independent claim 1,

"A method of operating a non-volatile memory. [Sekine discloses in column 1, line 13, "A flash memory is a non-volatile IC memory..."]

device driver [The MSCD defines “device driver” on page 155 as “a software component that permits a computer system to communicate with a device...” Sekine teaches a device driver, in column 7, lines 26-30.] *comprising: counting a number of write and/or erase* [Sekine discloses in column 1, lines 31-35, “In this patent specification, the present invention is explained in detail mainly with respect to the write function, but it can be similarly applied to the erase function of the flash memory as well.”] *access cycles to a non-volatile memory without regard to a failure of the write and/or erase access cycle; [disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.] and halting access to the non-volatile memory at a selected count.” [column 7, lines 19-21, “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.” Also see column 7, lines 35-40.]*

With respect to independent claim 11,

“A method of operating a system comprising: counting a number of write and/or erase access operations [Sekine discloses this limitation in column 1, lines 31-35]; to a Flash memory device [Sekine discloses in column 1, line 13, “A flash memory is a non-volatile IC memory...”]

coupled to a host [FIG. 1, element 20, "EWS"] without regard to a failure of the write and/or erase access operations[disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]; and stopping access execution to the Flash memory at a selected number of access operations." [column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test." Also see column 7, lines 35-40.]

With respect to independent claim 20,

"A method of testing a Flash memory [see Title of invention] comprising: counting a number of access operations to a Flash memory [disclosed e.g. in column 4, lines 42-45] for a Flash command without regard to a failure of altering a state of any memory cell of the Flash memory altered by the access operations [disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]; ["command" is disclosed in column 1, line 24] interrupting execution of the Flash command at a selected halt count of access operations, halting access to the Flash memory; [column 7, lines 19-21, "...when the writing test is repeated until the predetermined

maximum number of times, the process terminates and proceeds to the next test.”] and executing a power loss recovery cycle to test power loss recovery at the selected halt count.” [disclosed in column 6, lines 18-29 and column 1, lines 30-31, Sekine teaches test system which can monitor the voltage or power of the Flash memory driver at various intervals]

With respect to **independent claim 31**,

“A method of profiling a Flash command comprising: counting a number of access operations to a Flash memory during execution of [disclosed e.g. in column 4, lines 42-45] a Flash command without regard to a success or failure of the write and/or erase access operations; [Sekine discloses this limitation in column 1, lines 31-35. Also disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]] to create an access operation profile for the Flash command; [“command” is disclosed in column 1, line 24] and comparing the access operation profile two or more Flash commands.” [disclosed in column 1, lines 54-64]

With respect to **independent claim 33, and claim 38,**

"A system comprising: at least one Flash memory device; [Sekine discloses in column 1, line 13, "A flash memory is a non-volatile IC memory..."] and a host coupled to the at least one Flash memory device, [...engineering work station (EWS)..."] disclosed in column 1, line 64- column 2, line 4] wherein the host is adapted to count a number of write and/or erase access operations [Sekine discloses this limitation in column 1, lines 31-35] to the at least one Flash memory device during a Flash command without regard to a success or failure of the write and/or erase access operations [disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.] and halt execution of the Flash command, stopping access to the Flash memory device at a selected count of access operations." [column 2, lines 5-14 and column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test." Also see column 7, lines 35-40.]

With respect to **independent claim 40,**

"A machine-usable medium, [e.g. Flash memory module that stores a program] the machine-usable medium containing a software routine

[“software process....software procedure” disclosed in column 7, lines 29-34 for causing a processor to execute a method, [column 1, lines 20-23] wherein the method comprises: counting a number of write and/or erase access cycles [Sekine discloses this limitation in column 1, lines 31-35] to a Flash memory without reading any non-volatile memory cells written or erased by the write and/or erase access cycles[disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]; and halting execution at a selected count of write and/or erase access cycles, halting access to the Flash memory.” [Sekine further discloses in column 8, lines 38-50, “At least one or more data processing programs to perform the display process are stored in the DISK 21. Such programs include a condition set program to create a condition data file, a device test program...”]

With respect to independent claim 43,

“A system comprising: at least one Flash memory device; [Sekine discloses in column 1, line 13, “A flash memory is a non-volatile IC memory...”] and a host coupled to the at least one Flash memory device, [“...engineering work station (EWS)...” disclosed in column 1, line 64- column 2, line 4] “

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The following limitations of **claim 43** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant's specification in paragraph [0035], the Examiner notes that the means or system/structure ("**device driver**") for practice of the invention disclosed in the following limitation of Claim 35, is further taught in

Sekine as follows:

*"...wherein the host comprises a means for counting the number a number of write and/or erase access cycles [Sekine discloses this limitation in **column 1, lines 31-35**] to the at least one Flash memory device during execution of a Flash command without regard to a success or failure of the write and/or erase access cycles..." [disclosed e.g. in **column 1, lines 54-63**. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]*

According to the applicant's specification in paragraph [0037], the Examiner notes that the means or system/structure ("**device driver**") for practice of the invention disclosed in the following limitation of Claim 43, is further taught in

Sekine as follows:

"...and comprises a means for halting execution [...]"process terminates"] of the Flash command on the at least one Flash memory

device in response to the count of the access cycle counting means, stopping access to the Flash memory device.” [column 7, lines 19-21, “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.” Also see column 7, lines 35-40.]

Dependent Claims

With respect to **claim 2**,

“The method of claim 1, wherein the driver is a low level driver.” [The MSCD defines “device driver” on page 155 as “a software component that permits a computer system to communicate with a device...” Sekine teaches a device driver, in column 7, lines 26-30.]

With respect to **claims 21 and 32**,

“The method of claim 1, wherein counting the number of access cycles further comprises counting the number of write and/or erase cycles.” [disclosed e.g. in column 1, lines 7-10, “...counts the numbers of times of write or erase operations...” Also see column 1, lines 5-7]

With respect to **claims 5 and 16**,

“The method of claim 1, further comprising: restarting execution of the non-volatile memory command [“command” is disclosed in column 1,

line 24] *after halting execution at the selected count.”* **[column 7, lines 19-21,** “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.” The examiner notes that the next test can be the same as the previous test, thereby restarting the test.]

With respect to **claims 6 and 15,**

“The method of claim 1, further comprising: testing driver power loss recovery [disclosed in column 6, lines 18-29 and column 1, lines 30-31, Sekine teaches test system which can monitor the voltage or power of the Flash memory driver at various intervals] after halting execution access to the non-volatile memory at the selected count.” **[column 7, lines 19-21,** “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.” Different tests can be ran according to the user’s preference]

With respect to **claims 7, 25, and 42,**

“The method of claim 1, wherein halting access to the non-volatile memory at a selected count further comprises at a selected number of write and/or erase [see rejection to claim 1] access cycles, [column 7, lines 19-21, “...when the writing test is repeated until the predetermined

maximum number of times, the process terminates and proceeds to the next test.”] *counting the number of clock cycles and halting execution of the access cycle at a selected number of clock cycles.”* **["The timing generator 12 generates clock timing signals which determine the overall timings of the test system and sends the clock timing signals to the pattern generator 13.”]**

With respect to **claims 8, and 17,**

“The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles [column 7, lines 19-21], “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.”] *further comprises removing power from the non-volatile memory.”* **[disclosed in column 6, lines 18-29 and column 1, lines 30-31, Sekine teaches test system which can monitor the voltage or power of the Flash memory driver at various intervals]**

With respect to **claims 9, 18, and 29,**

“The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles [column 7, lines 19-21], “...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.”] *further*

comprises loading an internal register [internal register is interpreted by the examiner as "condition set program" disclosed in column 8, line 40] in the non-volatile memory and halting execution of a command execution logic of the non-volatile memory at the selected number of clock cycles." [column 7, lines 19-21]

With respect to **claims 10, 19, and 30,**

"The method of claim 7, wherein halting execution of the access cycle at a selected number of clock cycles [column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test."] further comprises loading an internal register [internal register is interpreted by the examiner as "condition set program" disclosed in column 8, line 40] in the non-volatile memory and halting execution of a command execution logic state machine [FIGs. 1, 3] of the non-volatile memory at a selected number of steps." [column 7, lines 19-21, "...the predetermined maximum number of times."]

With respect to **claim 13,**

"The method of claim 11, further comprising: examining a state ["fail analysis", column 7, line 21] of one or more host registers and/or the

memory device [flash memory] after stopping execution.” [column 7, lines 20-24, “...the process terminates...”]

With respect to claim 14,

“The method of claim 11, further comprising: rebooting the host [FIG. 1, element 20, “EWS”] after stopping access execution to the Flash memory.” [It is notoriously well known to anyone of ordinary skill in the art that a workstation or host can be rebooted after stopping execution.]

With respect to claims 22 and 27,

“The method of claim 20, further comprising: changing the selected halt count; [column 7, lines 19-21 “...when the writing test is repeated until the predetermined maximum number of times...”] re-executing the Flash command; [column 7, lines 19-21 “...the process terminates and proceeds to the next test.”] counting a number of access operations; [disclosed e.g. in column 4, lines 42-45] and interrupting execution of the Flash command at the changed halt count.” [column 7, lines 19-21, “...the process terminates and proceeds to the next test.”]

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With respect to **claims 23 and 28**,

"The method of claim 22, wherein changing the selected halt count ["...when the writing test is repeated until the predetermined maximum number of times..."] further comprises incrementing the selected halt count." [column 7, lines 19-21. Sekine teaches that the predetermined maximum number of times (halt count) can be changed or incremented.]

With respect to **claim 24**,

"The method of claim 22, further comprising: changing the Flash command after all possible halt counts of the Flash command have been tested." [column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test."]

With respect to **claims 26 and 39**,

"The method of claim 25, wherein interrupting execution of the access operation at a selected number of clock cycles [column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test."] further comprises triggering external hardware [disclosed

e.g. in column 1, line 64 – column 2, line 4] to remove power from the Flash memory.”

With respect to **claim 37**,

“The system of claim 33, wherein the host [“...**engineering work station (EWS)**...” disclosed in column 1, line 64- column 2, line 4] is one of a processor and an external memory controller.” [disclosed in column 6, lines 18-22, “In FIG. 1, the flash memory test system includes an engineering work station (EWS) 20 with a large capacity storage DISK 21 and a test processor 11 both of which are connected to a tester hardware through a tester bus.”]

With respect to **claim 44**,

“The system of claim 43...”

The following limitations of **claim 44** are interpreted under 35 U.S.C. 112, 6th paragraph.

According to the applicant’s specification in paragraph [0035], the Examiner notes that the means or system/structure (“**device driver**”) for practice of the invention disclosed in the following limitation of Claim 35, is further taught in

Sekine as follows:

“...wherein the host comprises a means for counting the number of access cycles [disclosed e.g. in column 4, lines 42-45] to the at least one Flash

memory device during execution of a Flash command... [**"command" is disclosed in column 1, line 24 [NOTE: The examiner interprets device driver as "data processing programs" disclosed by Sekine in column 8, line 38.]**

According to the applicant's specification in paragraph [0037], the Examiner notes that the means or system/structure ("**device driver**") for practice of the invention disclosed in the following limitation of Claim 43, is further taught in

Sekine as follows:

"...and comprises a means for halting execution [...]"process terminates"] of the Flash command on the at least one Flash memory device in response to the count of the access cycle counting means."
[column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test."]

"...when a means for timing the execution of a last access cycle has elapsed." [**"...predetermined maximum number of times..." disclosed in column 7, lines 19-21**]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere CO.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims **35** and **36** are rejected under 35 U.S.C. 103(a) as being obvious over Sekine (U.S. Patent no. 5,896,398) in view of Kim (US PG Pub No. 2003/0075609 hereafter referred to as Kim).

With respect to claim 35, Sekine teaches "*wherein the at least one Flash memory device ...*" as shown in column 1, lines 1-12. With respect to claim 36, Sekine teaches "*wherein an interface to the Flash memory device ...*" as shown in FIG.1.

Sekine, however, does not disclose *expressly* "...is one of a NAND Flash and a NOR Flash" of claim 35. Sekine also does not disclose *expressly* "...is one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, MemoryStick, Secure Digital Memory Card, and a multimedia card (MMC) compatible interface" of claim 36.

With respect to claim 35, Kim discloses in paragraph [0019], "...NAND-type flash memory." With respect to claim 36, Kim discloses in paragraph 0005, "...a memory card such as an SMC (Smart Media Card) and MMC (Multimedia Memory Card)."

Sekine and Kim are analogous art because they are from the same field of endeavor, that being memory card or flash memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a flash memory as a NAND-type flash memory because flash memory is usually implemented as either NOR or NAND-type. Also at the time of invention it would have been obvious to a person of ordinary skill in the art to incorporate a flash memory as an MMC in order to interface with MMC readers.

The motivation for doing so would have been obvious based on the teaching of Kim in paragraph [0006], "A memory card based on a flash memory recently developed is very popular due to the card's high capability of data transmission."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Sekine and Kim before him/her to combine Kim and Sekine for the benefit of having a NAND-type flash memory implemented as an MMC to obtain the inventions as specified in claims 35 and 36.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS**POINT OF ARGUMENT for Claim 1:**

With respect to the arguments on pages 9-11 of the applicant's remarks, the examiner acknowledges the applicant's arguments with regard to the differences in teachings of Sekine and the applicant. However, the examiner maintains his stance on the rejection of claim 1 because the applicant's *claim language* is taught by the prior art of reference. As interpreted by the examiner the following claim limitations are taught by the prior art: *comprising: counting a number of write and/or erase* [Sekine discloses in column 1, lines 31-35, "In this patent specification, the present invention is explained in detail mainly with respect to the write function, but it can be similarly applied to the erase function of the flash memory as well."] *access cycles to a non-volatile memory without regard to a failure of the write and/or erase access cycle*; [disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.] *and halting access to the non-volatile memory at a selected count.*" [column 7, lines 19-21, "...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test." Also see column 7, lines 35-40.] The examiner has cited different elements within Sekine that anticipate the

applicant's instant amendments. Furthermore, the examiner maintains the previous arguments with respect to the applicants arguments on page 11 of the instant remarks.

POINT OF ARGUMENT for Claim 11, 20, and 31:

With respect to the arguments on page 12 of the applicant's remarks, the examiner acknowledges the applicant's arguments with regard to the differences in teachings of Sekine and the applicant. However, the examiner maintains his stance on the rejection of claim 11 because the applicant's *claim language* is taught by the prior art of reference.

POINT OF ARGUMENT for Claim 33, 40, and 43:

With respect to the arguments on page 11 of the applicant's remarks, the examiner acknowledges the applicant's arguments with regard to the differences in teachings of Sekine and the applicant. However, the examiner maintains his stance on the rejection of claim 33 because the applicant's *claim language* is taught by the prior art of reference.

POINT OF ARGUMENT for Claims 35 and 36

Discussed supra in the argument to claim 33. As such, the rejection stands to claims 35 and 36.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

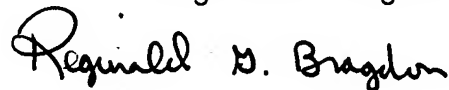
Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have

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questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon

A handwritten signature in black ink that reads "Reginald G. Bragdon". The signature is written in a cursive style with a large initial "R".

HLF
February 5th, 2007

Supervisory Patent Examiner
Technology Center 2100